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An Efficient Design of Frame Synchronization in FPGA

01/05/2015 · Sri Ventakeshwara College of Engineering, Chittoor Y Murali Mohan Babu, PhD, MTech Professor, Sri Ventakeshwara College of Engineering, Chittoor Frame synchronization is obtained by inserting in series (eg at the beginning of each frame), or in parallel (ie on a separate sync channel), a frame sync code (FSC)

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common example of full-duplex communication is the telephone network When two people are communicating by a telephone line, both can talk and listen at the same time The full-duplex mode is used when communication in both directions is required all the time The capacity of the channel, however, must be divided between the two directions

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